

Multi-edge type LDPC codes

Tom Richardson

On the occasion of Bob McEliece's
60th birthday celebration





Vector-Low-Density Parity-Check™ (V-LDPC™) Coding Solution Data Sheet

High Speed, High Performance Advanced Forward-Error Correction (FEC) Intellectual Property (IP) Cores

Overview

The Vector-LDPC™ Coding Solution consists of a scalable family of high-speed Low-Density Parity-Check (LDPC) encoders and decoders in the form of an intellectual property (IP) core that can be used in communication systems requiring Forward Error Correction (FEC). The code rate and design are programmable and changeable on-the-fly. The scalable architecture can support a wide range of throughputs (up to 10Gbps) and a variety of design requirements.

Vector-LDPC™ codes have been successfully implemented in Flarion's Basestream™ system for mobile wireless communications systems.

Low-density parity-check (LDPC) codes are a class of binary linear error-correcting

codes that can be decoded by an iterative soft-in, soft-out (ISI) decoding algorithm. Flarion has developed a powerful architecture for LDPC codes, allowing for high-speed performance and programmable LDPC code designs, yielding significant advantages over Turbo Codes and other FEC implementations.

Vector-LDPC™ codes beat out Turbo Codes in performance, with less hardware complexity, higher throughput, more flexibility and lower error floors.

LDPC codes offer superior coding gain exceeding that of Turbo Codes. They can be designed to have very low error floors, eliminating the need for an outer Reed-Solomon code. The Vector-LDPC™ solution supports fully programmable LDPC code designs, allowing customization for each application.

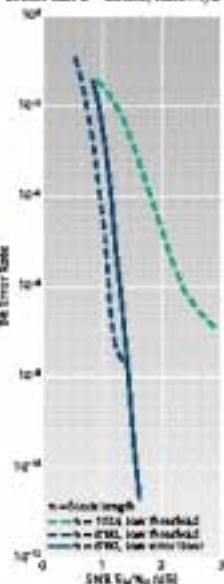
Flarion's parallel architecture enables the efficient encoding and decoding of LDPC codes, making the Vector-LDPC™ solution well suited for high-speed applications.

Many high-speed communications applications stand to benefit from the large coding gains, high data rate, and smaller hardware size of these IP cores.

Applications

- Optical Fiber Communications
- Satellite (digital video and audio broadcast)
- Storage (magnetic, optical, holographic)
- Wireless (mobile, fixed)
- Wireline (cable modems, DSL)

Vector-LDPC™ Codes, Rate=1/2



Vector-LDPC™ Solution

- LDPC Encoder Core
- LDPC Decoder Core

Selected Features

- Efficient encoding algorithm
- Optimized LDPC code designs and minimal quantization loss yield near-capacity performance
- "Soft-in, soft-out" decoder compatible with turbo equalization
- Compatible with various modulation formats (QPSK, QAM)
- Early detection of convergence
- Improved average throughput due to statistical multiplexing buffers

Flexibility

- Highly parallel and scalable
- Supports a wide range of data speeds and hardware sizes
- Programmable coding rates and flexible block lengths
- Firmware allows downloading and test swapping of LDPC codes
- LDPC codes are optimized for low error floors, large coding gains, high speed, etc.

Deliverables

- VHDL netlist
- VHDL test bench and test vectors
- Documentation
- C++ and MATLAB software models
- LDPC code designs
- Support and maintenance contract

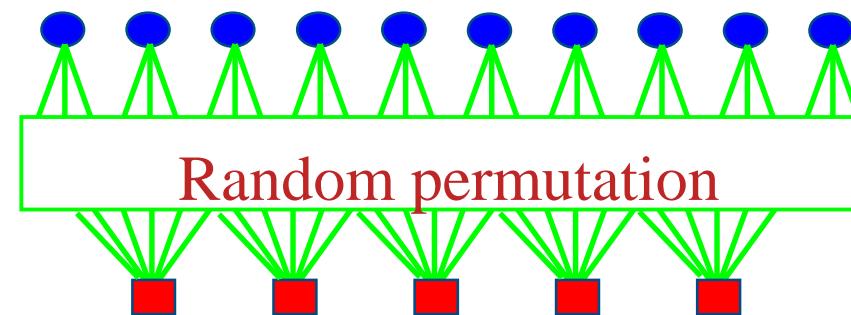


Outline

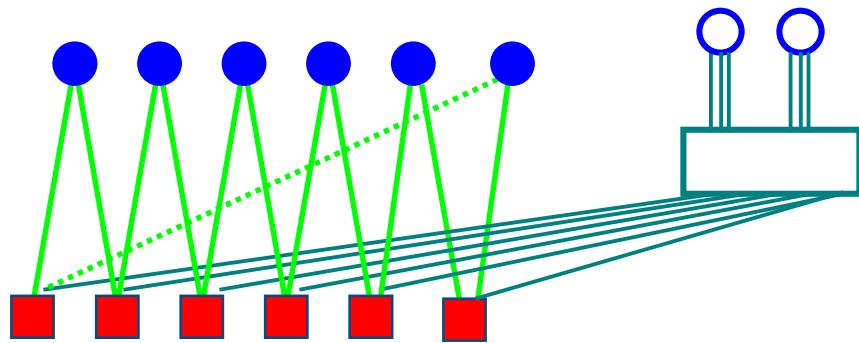
- Codes: New and improved LDPC codes.
- Error Floors: The final frontier.
- Turbo Equalization for noncoherent OFDM:
Structural constraints.



1961 R. Gallager



Multi-edge-type ensembles: RA

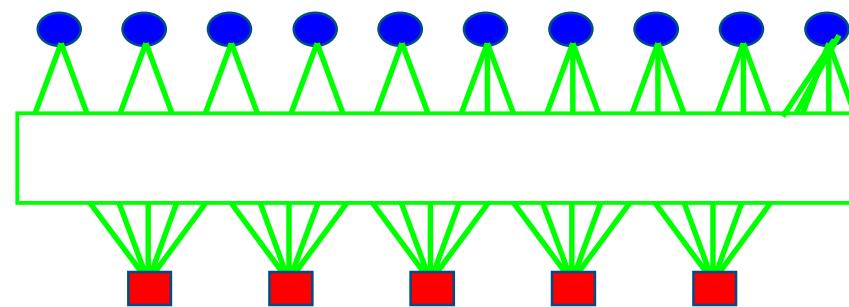


RA codes

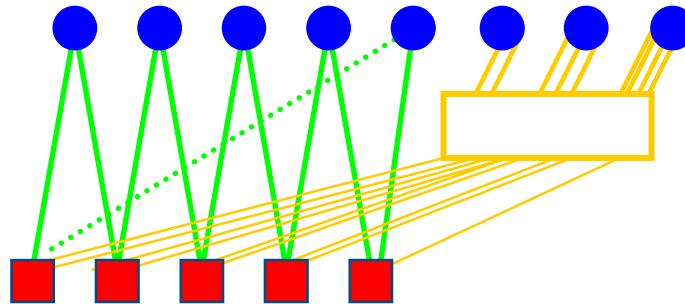
Divsalar, Jin, McEliece 1998



**1998
Irregular LDPC**



Multi-edge-type ensembles: IRA

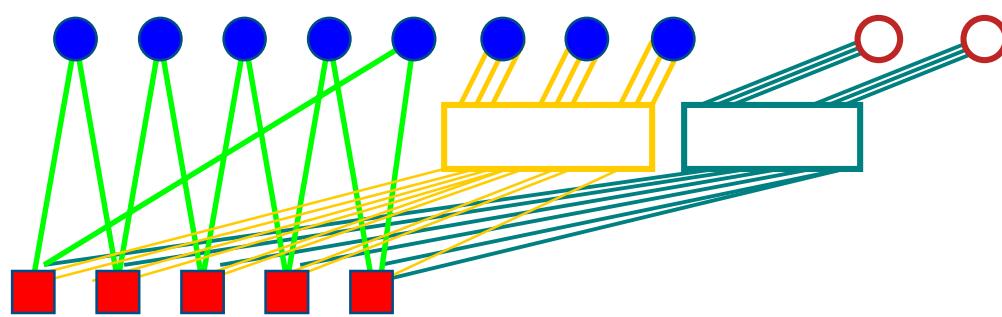


IRA codes

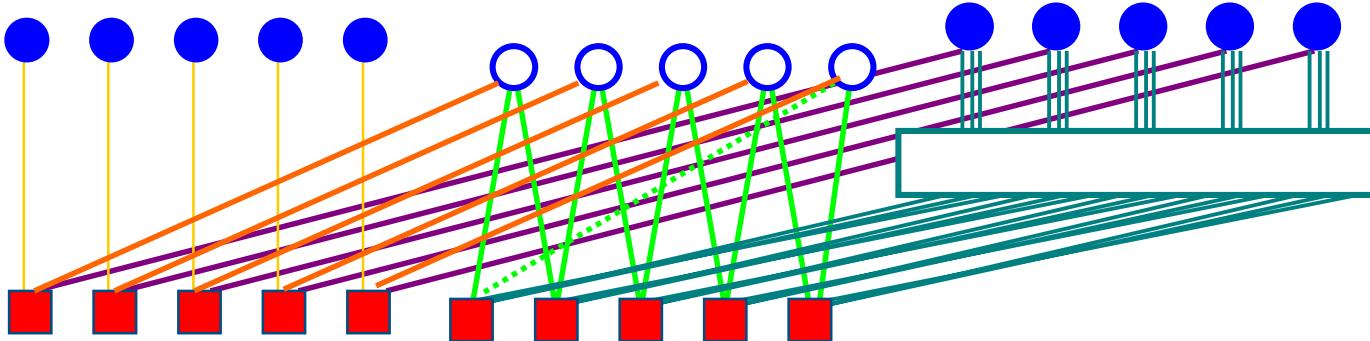
Jin, Khandekar, McEliece 2000



IRA + RA



Multi-edge-type ensembles: CT



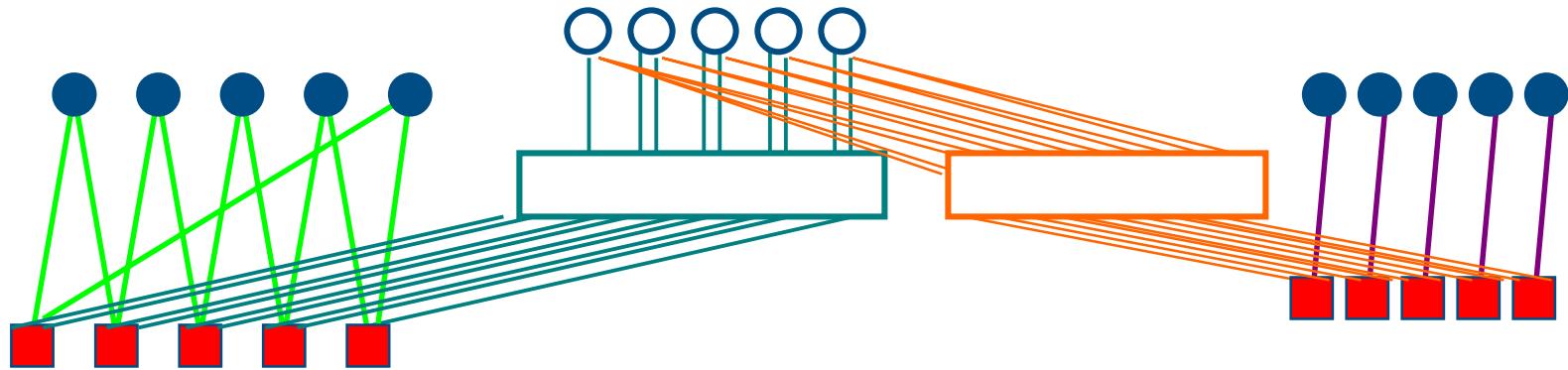
CT codes

Ping, Wu 2001

AWGNC threshold: 0.925



Multi-edge-type ensembles: MN

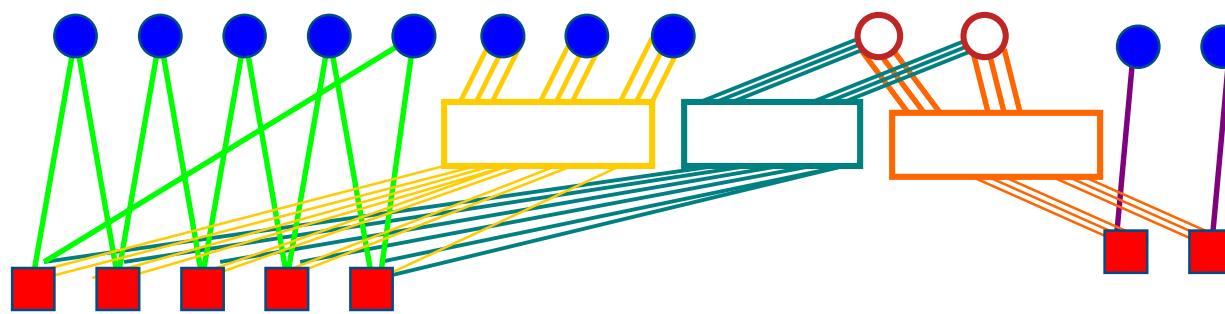


Kantor, Saad 2000

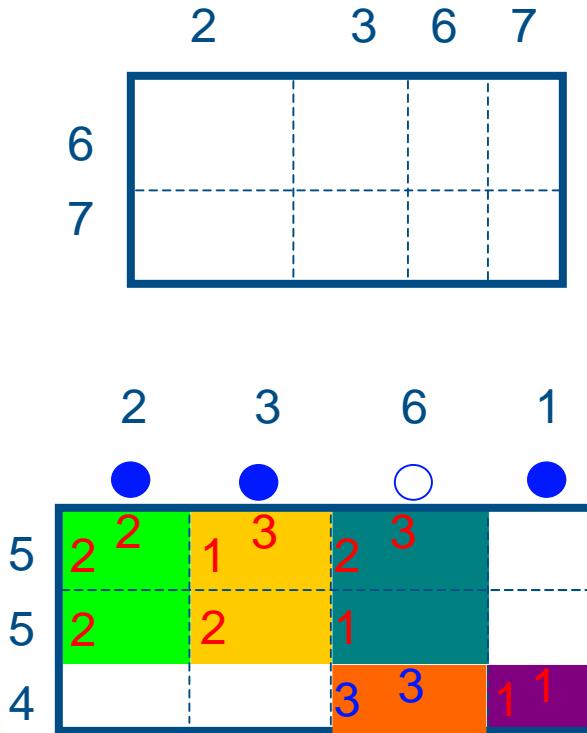
AWGNC threshold: ~ 0.95



IRA + RA + ... = Multi-edge type LDPC codes



Multi Edge Type LDPC codes: Parity check matrix perspective



Standard irregular LDPC:
specify row and column weights

Multi-edge type LDPC:
node type = column and row
clustering
received distribution specs.

Edge type specifies row and
column weights in any,
possibly disconnected,
rectangle.



Multi Edge Type LDPC codes:

Node perspective multivariate polynomial representation.

Standard irregular LDPC edge-perspective
degree polynomials.

$$\lambda(x), \rho(x)$$

Density Evolution: $F_{l+1} = R \lambda(\rho(F_l))$



Multi Edge Type LDPC codes:

Node perspective multivariate polynomial representation.

Edge types: $\mathbf{x}=(x_1, x_2, \dots, x_k)$; Densities: $\mathbf{F}=(F_1, F_2, \dots, F_k)$

received types: $\mathbf{r}=(r_1, r_2, \dots, r_l)$; Densities: $\mathbf{R}=(R_1, R_2, \dots, R_l)$

Degrees: $\mathbf{d}=(d_1, d_2, \dots, d_k)$, $\mathbf{b}=(b_1, b_2, \dots, b_l)$

$$x^{\mathbf{d}} = \prod_i x_i^{d_i}, \quad r^{\mathbf{b}} = \prod_i r_i^{b_i}$$



Node perspective multivariate polynomial representation.

$$v(r, x) = \sum v_{b,d} r^b x^d, \quad \mu(x) = \sum \mu_d x^d$$

Coefficients: $v_{b,d} n$ = #variable nodes of type b,d
 $\mu_d n$ = #check nodes of type d
where n is the blocklength

Edge equality constraints: $v_{x_i}(1,1) = \mu_{x_i}(1)$, $i=1,\dots,k$

Received constraints: $v_{r_i}(1,1) = \pi_i$, $i=1,\dots,l$

Code Rate: $v(1,1) - \mu(1)$



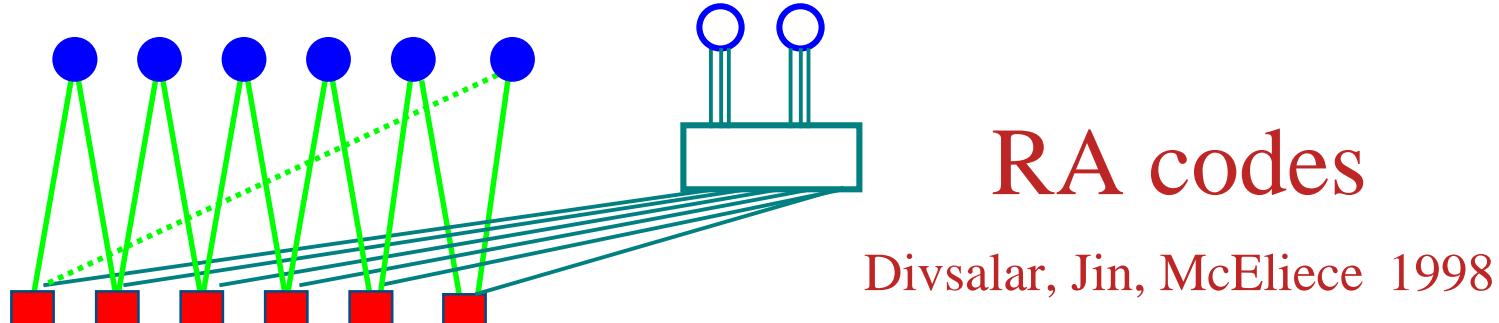
Node perspective multivariate polynomial representation.

The multi-edge formalism can be used to specify a particular graph. The formalism is, in this sense, universal.

The purpose, however, is to find good structures, i.e., ensembles.



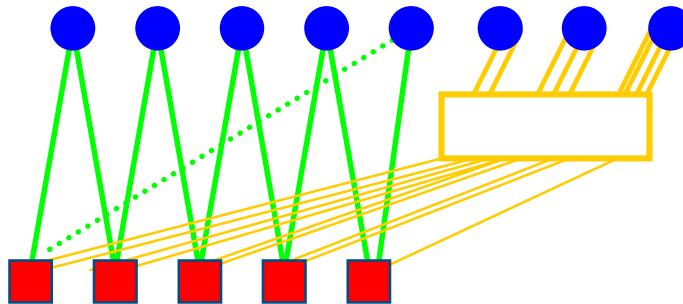
Multi-edge-type ensembles: RA



Variables			Constraints	
$v_{b,d}$	b	d	μ_d	d
$1/q$	1 0	$q \ 0$	1	1 2
1	0 1	0 2		



Multi-edge-type ensembles: IRA



IRA codes

Jin, Kandekkar, McEliece 2000

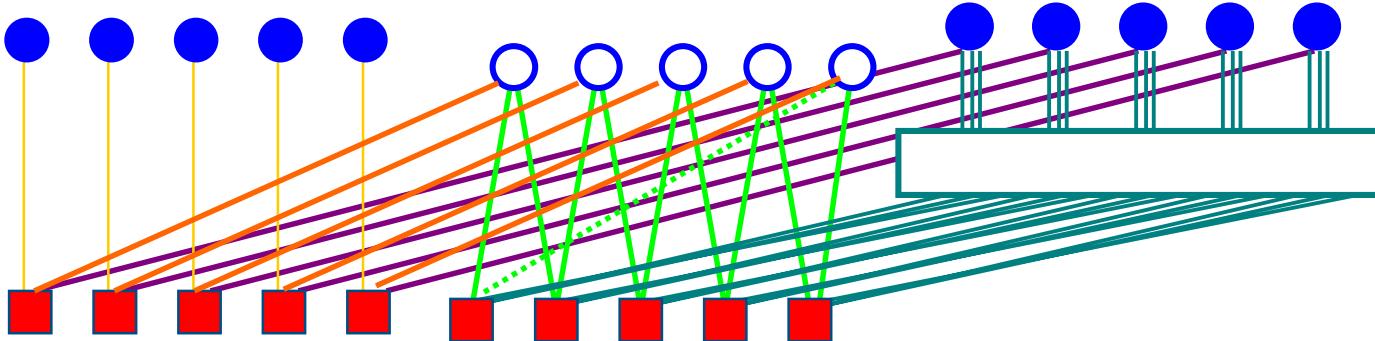
Variables			Constraints	
$v_{b,d}$	b	d	μ_d	d
0.33821	0 1	3 0	0.5	8 2
0.02910	0 1	11 0		
0.10805	0 1	12 0		
0.02980	0 1	48 0		
0.50000	0 1	0 2		

AWGNC threshold: 0.963

Shannon: 0.979



Multi-edge-type ensembles: CT



Variables			Constraints		
$v_{b,d}$	b	d	μ_d	d	
1/2	0 1	3 1 0 0 0	1/2	3 0 2 0 0	
1/2	1 0	0 0 2 1 0	1/2	0 1 0 1 1	
1/2	0 1	0 0 0 0 1			

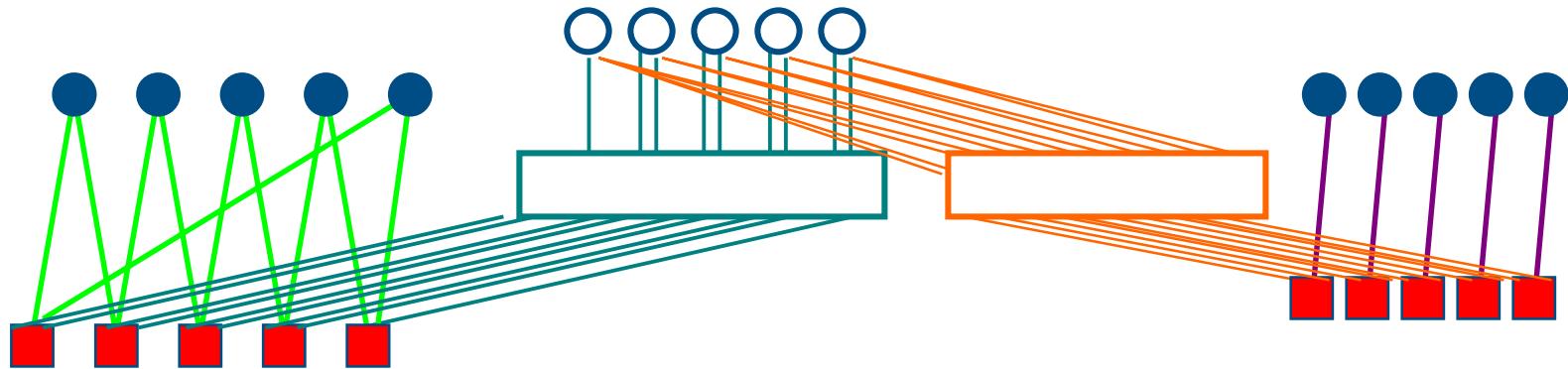
CT codes

Ping, Wu 2001

AWGNC threshold: 0.925



Multi-edge-type ensembles: MN



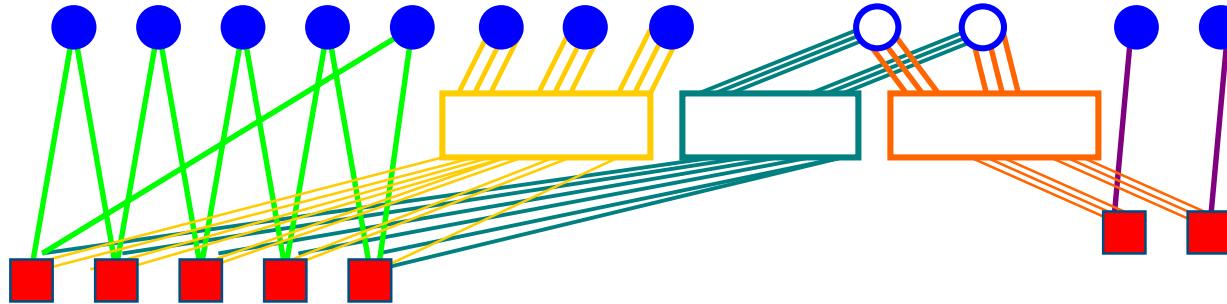
Variables			Constraints		
$v_{b,d}$	b	d	μ_d	d	
0.45	1 0	2 3 0 0	0.05	1 0 2 0	
0.05	1 0	1 4 0 0	0.45	2 0 2 0	
0.5	0 1	0 0 2 0	0.075	0 6 0 1	
0.5	0 1	0 0 0 1	0.05	0 7 0 1	
			0.375	0 2 0 1	

AWGNC threshold: ~ 0.95

Kantor, Saad 2000



Multi-edge-type ensembles

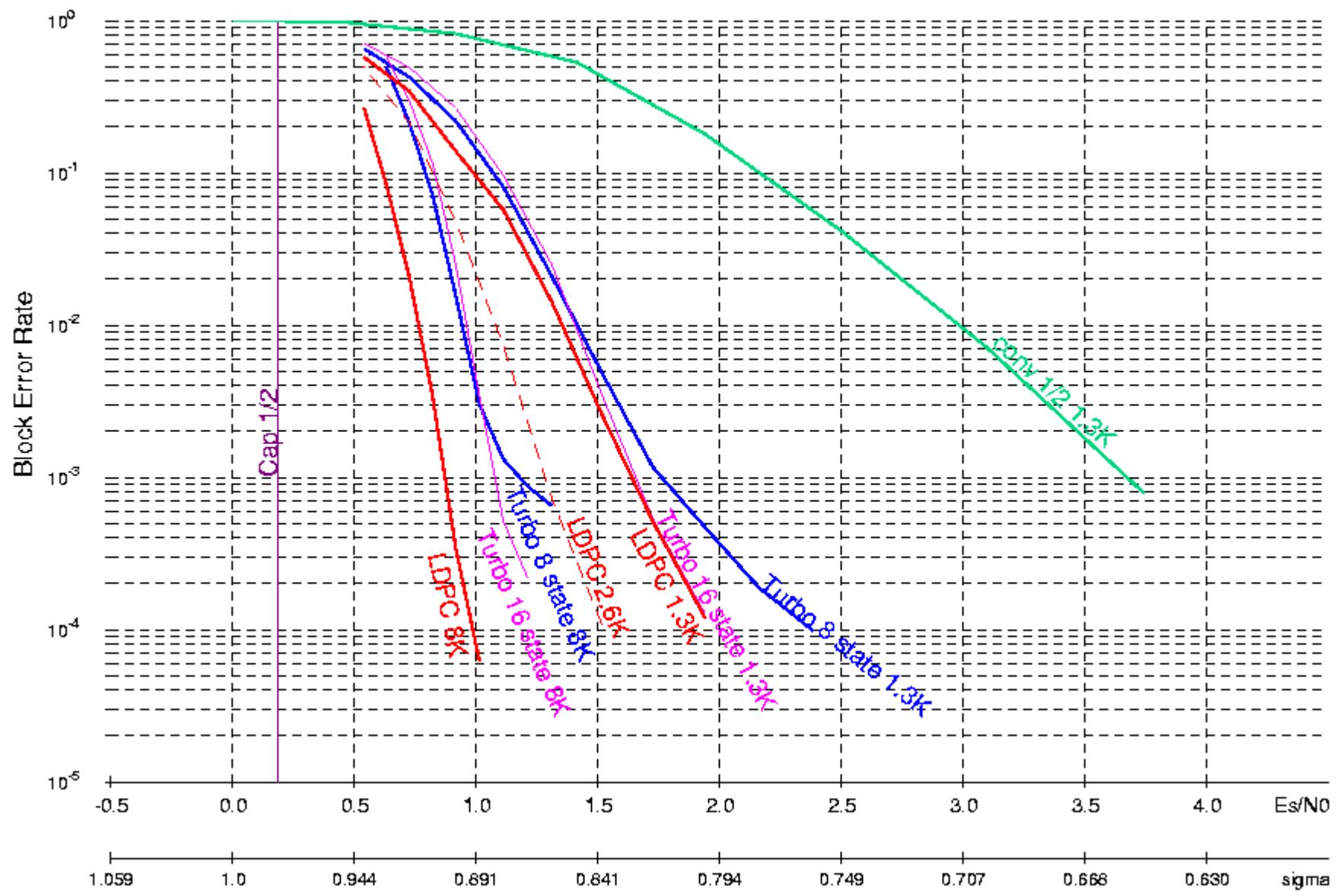


Variables			Constraints	
$v_{b,d}$	b	d	μ_d	d
0.5	0 1	20000	0.4	22100
0.3	0 1	03000	0.1	21200
0.2	1 0	00330	0.2	00031
0.2	0 1	00001		

AWGNC threshold: ~ 0.965



Performance



Multi Edge Type LDPC codes:

Node perspective multivariate polynomial representation.

$$\lambda(r, x) := \left(\frac{v_{x_1}(r, x)}{v_{x_1}(1, 1)}, \dots, \frac{v_{x_k}(r, x)}{v_{x_k}(1, 1)} \right)$$

$$\rho(x) := \left(\frac{\mu_{x_1}(x)}{\mu_{x_1}(1)}, \dots, \frac{\mu_{x_k}(x)}{\mu_{x_k}(1)} \right)$$

Density Evolution: $F_{l+1} = \lambda(R, \rho(F_l))$



Multi Edge Type LDPC codes:

Stability

Perfectly decodable fixed point.

$$F^* = \lambda (R, \rho (F^*))$$

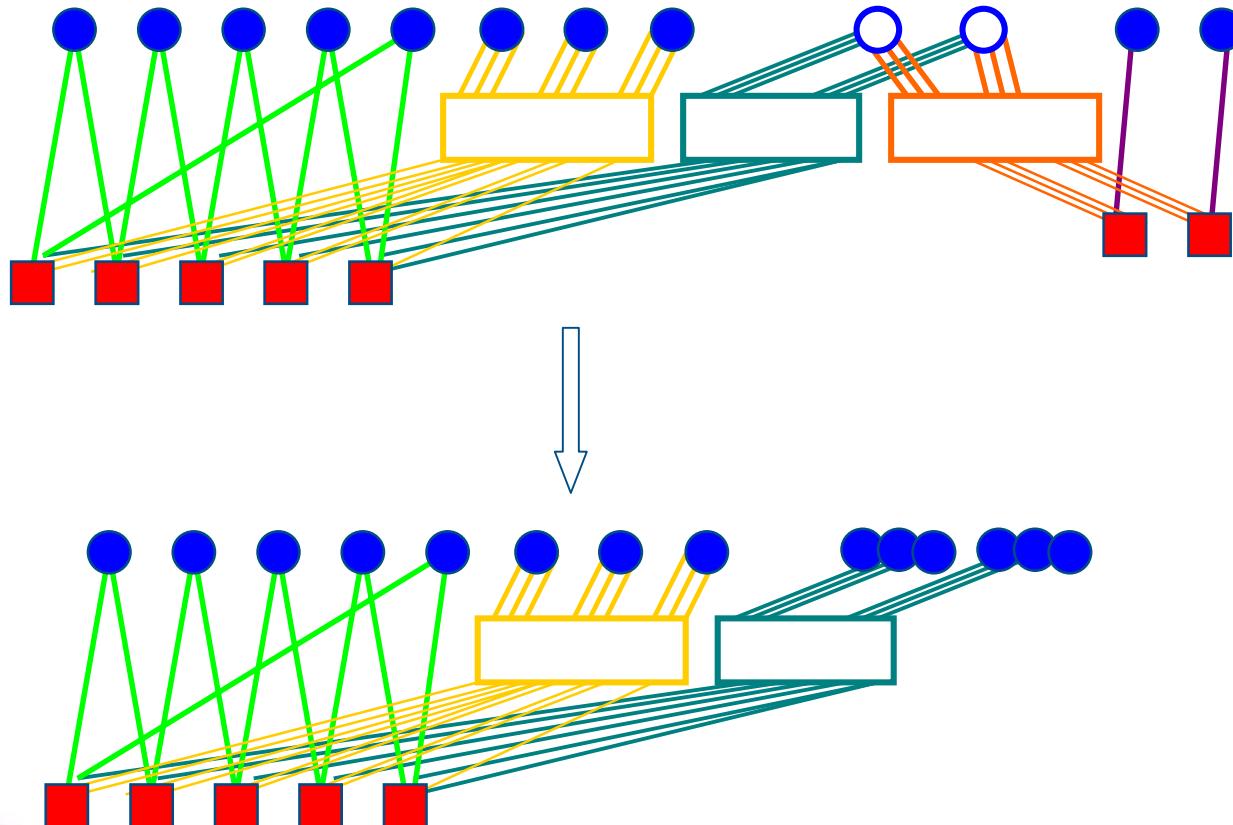
When is it stable ?

i.e., If $F_0 \approx F^*$ then does $F_1 \rightarrow F^*$?



Stability: Removal of Degree 1 nodes

Reduction to case $F^* = \delta_\infty$



Multi Edge Type LDPC codes:

Stability (Degree 1 nodes removed)

$$\Lambda_{i,j} := \frac{d}{dx_j} \lambda_i(\vec{r}, \vec{x}) \mid_{\vec{x}=0} \quad \quad \quad \mathcal{P}_{i,j} := \frac{d}{dx_j} \rho_i(\vec{x}) \mid_{\vec{x}=\vec{1}}$$

Stability Matrix: $\Lambda(\mathcal{B}\vec{R}) \mathcal{P}$

$$\mathcal{B}(P) := \int_{-\infty}^{+\infty} e^{-\frac{1}{2}x} P(x) dx$$



Multi Edge Type LDPC codes:

Stability : Examples

Standard Irregular LPDC: $\lambda_2 B(R) \rho'(1)$

Irregular RA code:

$$B(R) \begin{bmatrix} \frac{2\nu_{2,0}}{\nu_{x_1}} & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \frac{\mu_{x_1,x_1}}{\mu_{x_1}} & \frac{\mu_{x_2,x_1}}{\mu_{x_1}} \\ \frac{\mu_{x_1,x_2}}{\mu_{x_2}} & 1 \end{bmatrix}$$

$$= B(R) \begin{bmatrix} 0 & 0 \\ c & 1 \end{bmatrix} \quad \text{If } \nu_{2,0}=0$$



Error Floors

C. Di, D. Proietti, R. Urbanke, A. Shokrollahi,
E. Teletar



Error floors on the erasure channel: Stopping sets.

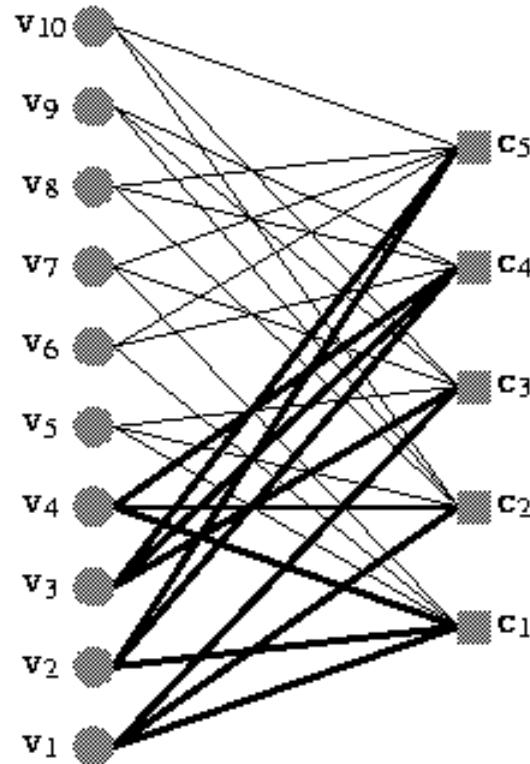


FIG. 3. The set $\{v_1, v_2, v_3, v_4\}$ is a stopping set.



Error floors on the erasure channel: average performance.

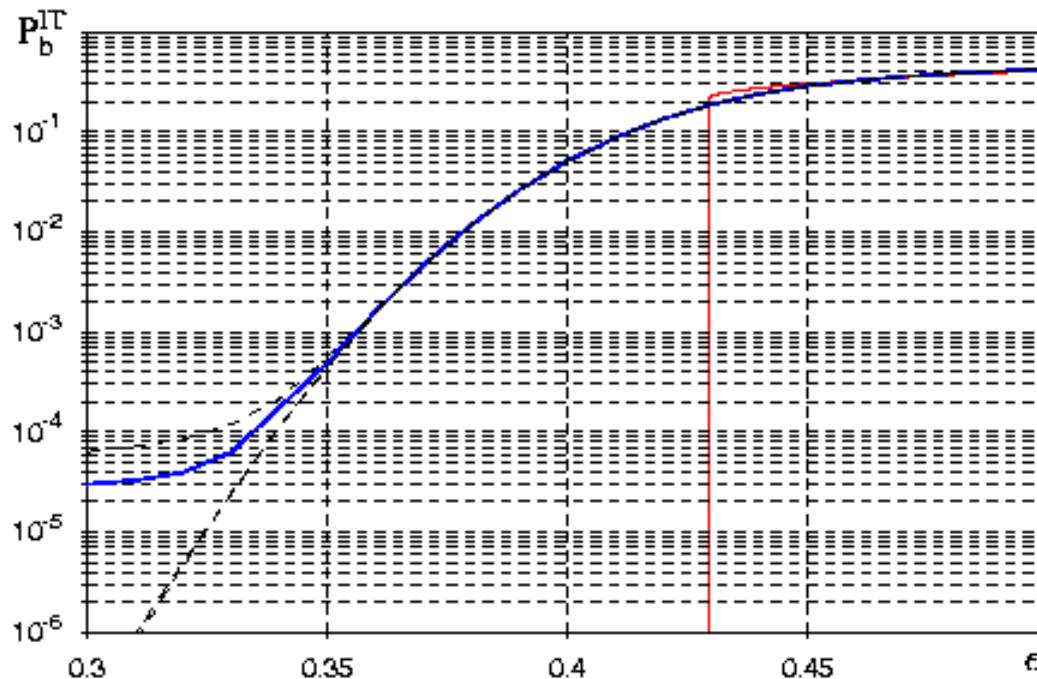


FIG. 1. Concentration of the bit erasure probability $P_b^{II}(G, \epsilon)$ for specific instances $G \in C(512, x^2, x^5)$ (dashed curves) around the ensemble average $E_{C(512, x^2, x^5)}[P_b^{II}(G, \epsilon)]$ (left solid curve). (It is noteworthy that there appear to be two dominant modes of behavior.) Also shown is the performance of the cycle-free case, $E_{C(\infty, x^2, x^5)}[P_b^{II}(G, \epsilon)]$ (right solid curve).

Error floors on the erasure channel: decomposition

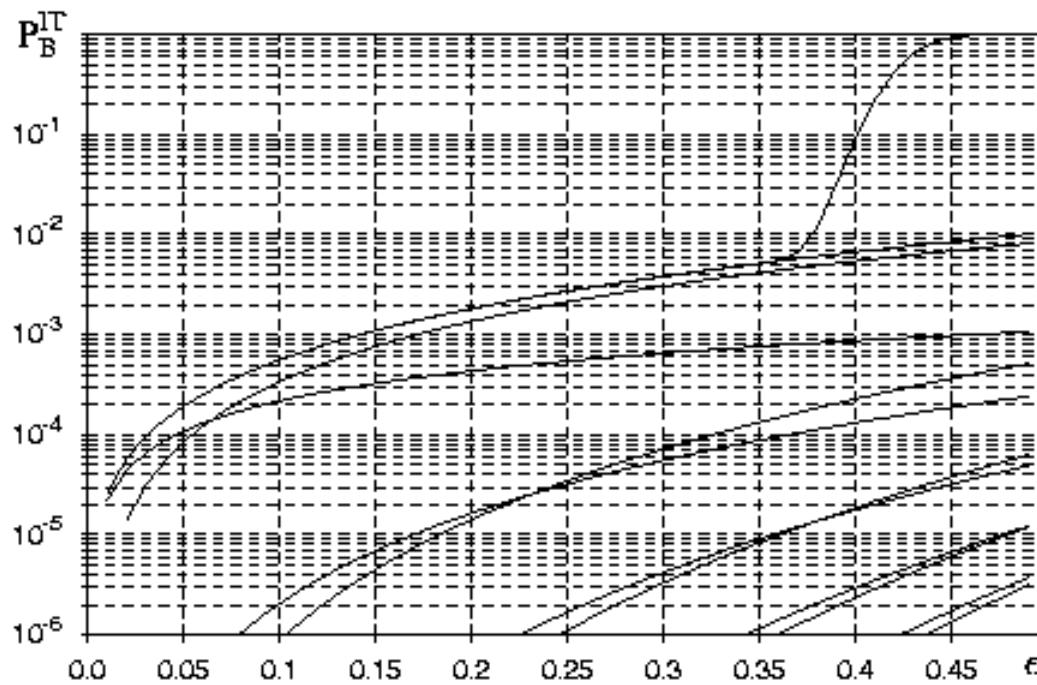
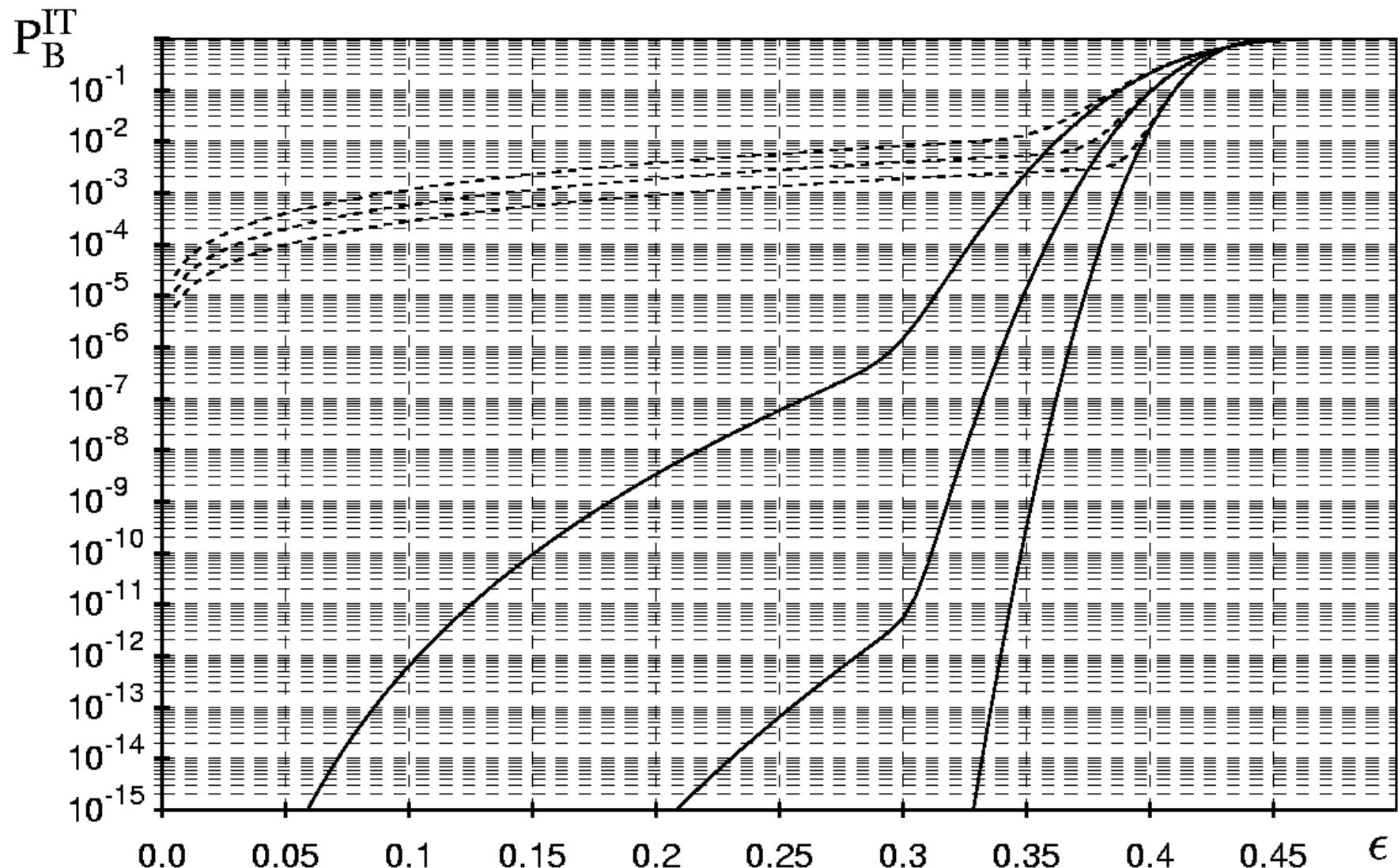


FIG. 1. *The contribution to the block error probability of stopping sets of size up to ten as estimated by the union bound.*



Error floors on the erasure channel: average and typical performance.



Error floors for general channels:

Stopping sets are no longer sufficient.

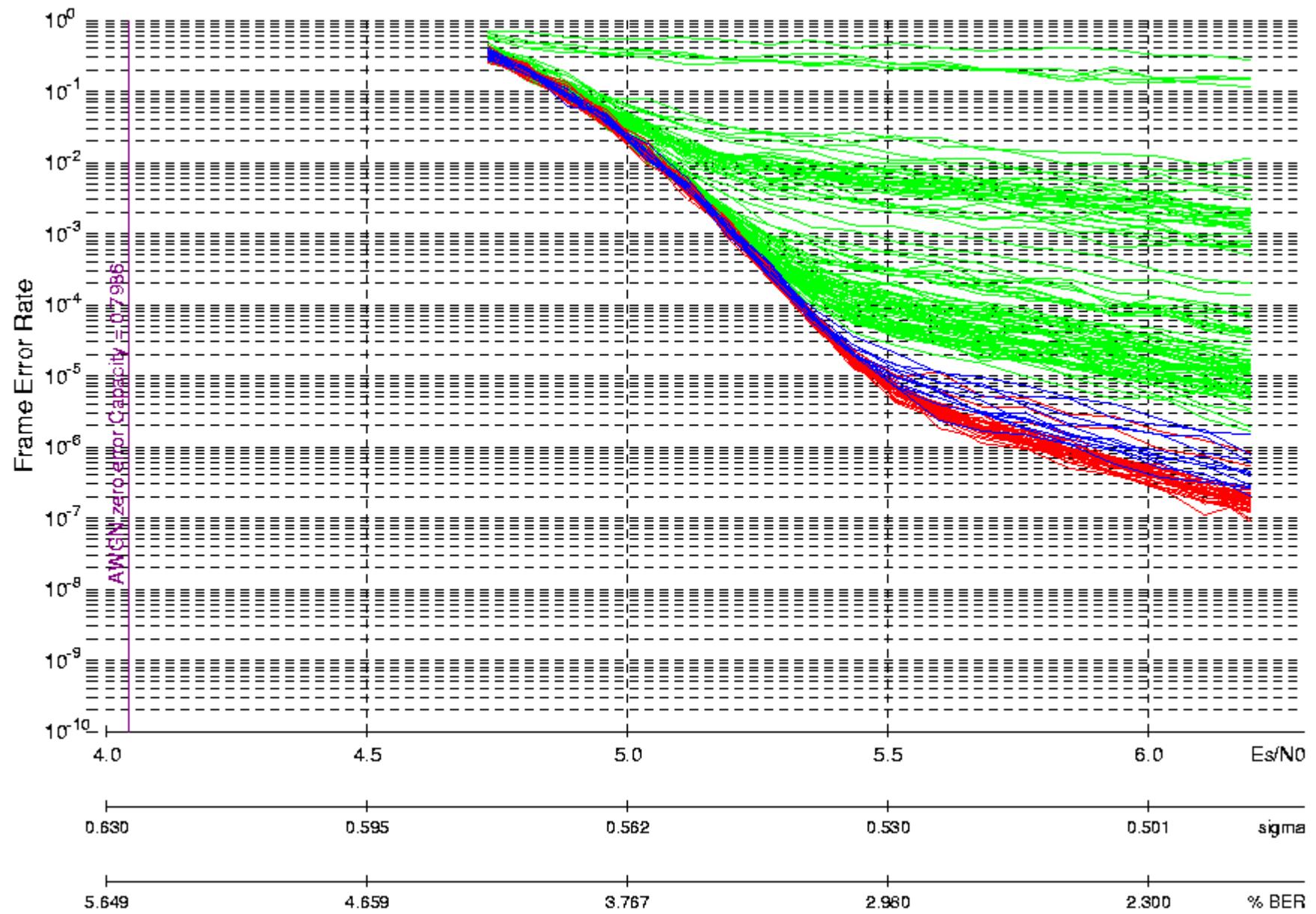
A generalization is required.

We know what that generalization is from experiments and other considerations.

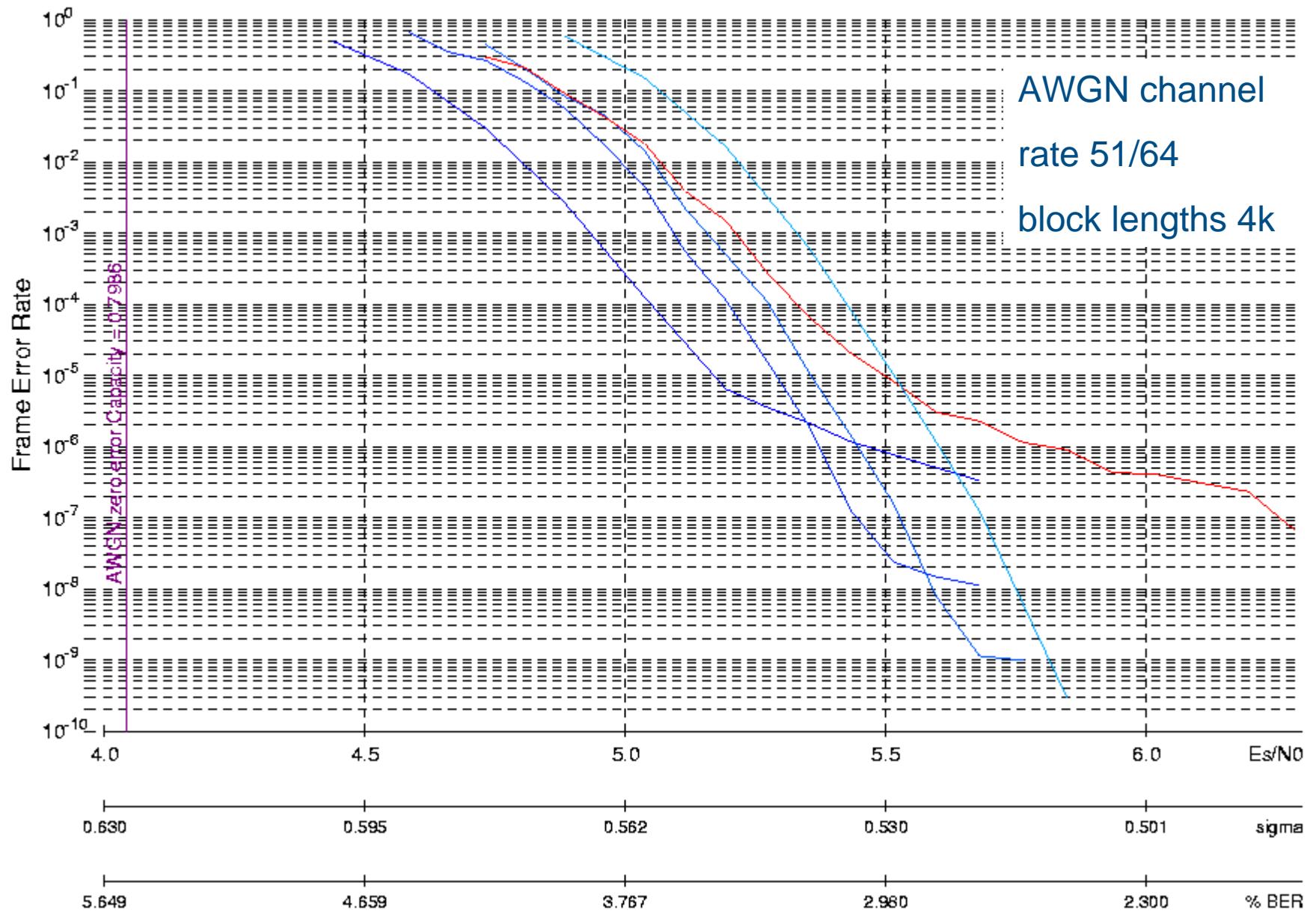
Combinatorial analysis, probabilistic analysis and simulation will yield accurate predictor.



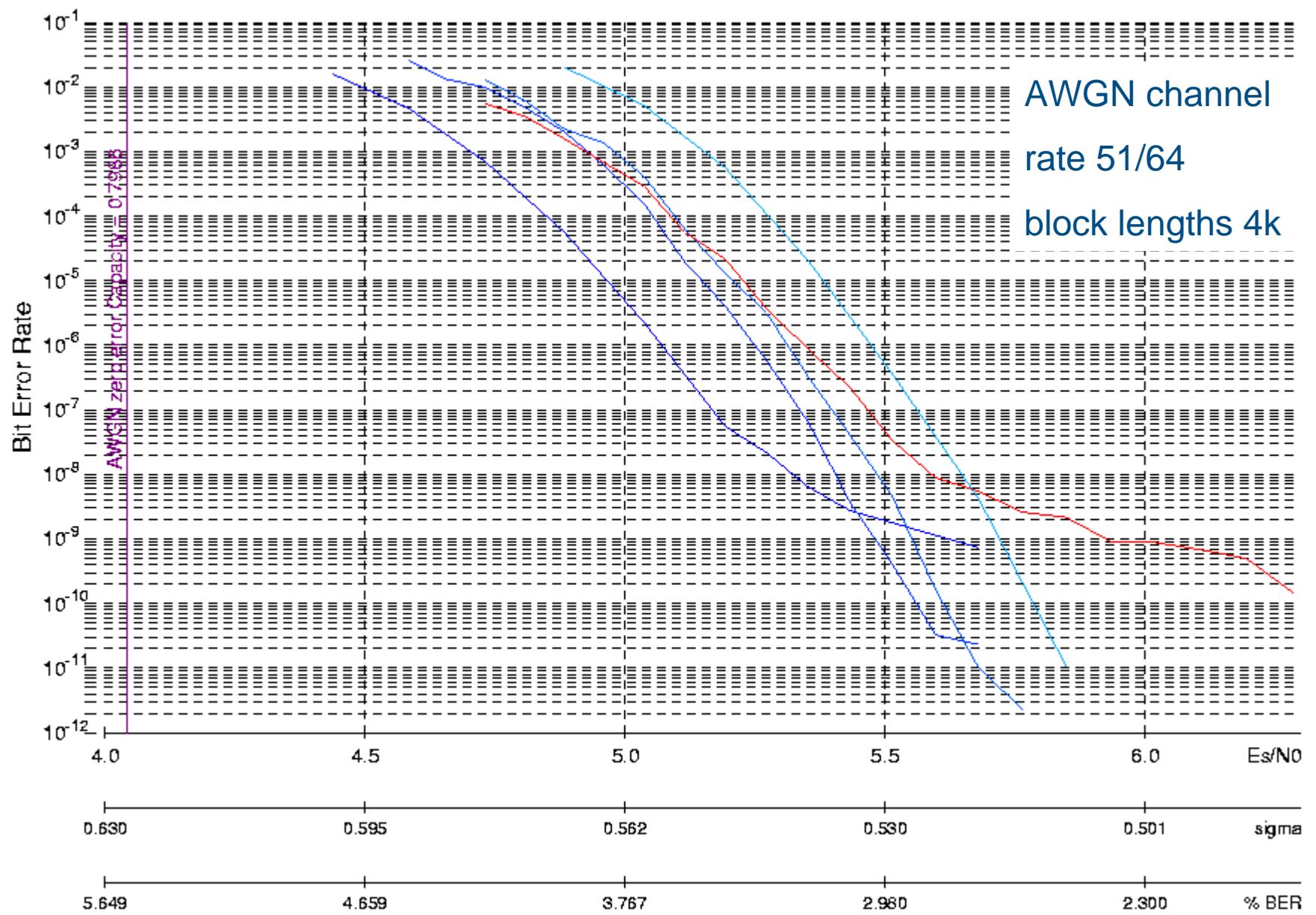
Error floors for general channels: Design example.



Error floors for general channels: Design example.



Error floors for general channels: Design example.



Turbo Equalization

Hui Jin



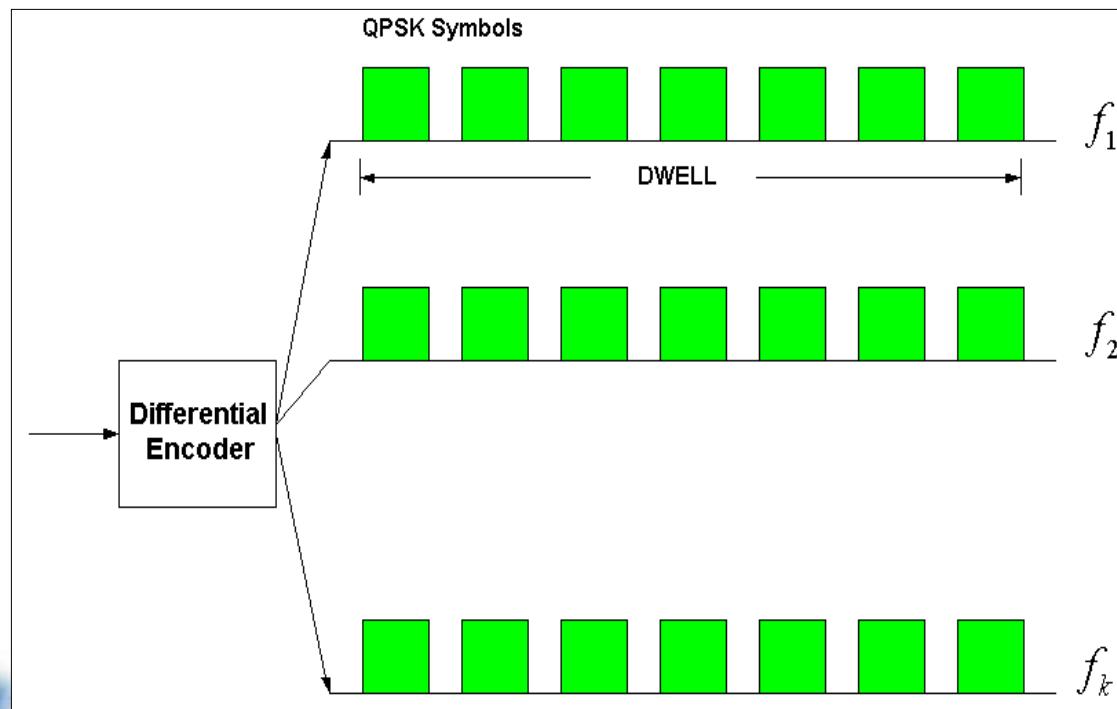
Turbo Equalizer for Noncoherent MPSK Communication

- Flarion Uplink System
- Design of LDPC codes in conjunction with turbo equalizer
- Hardware implementation of turbo equalizer

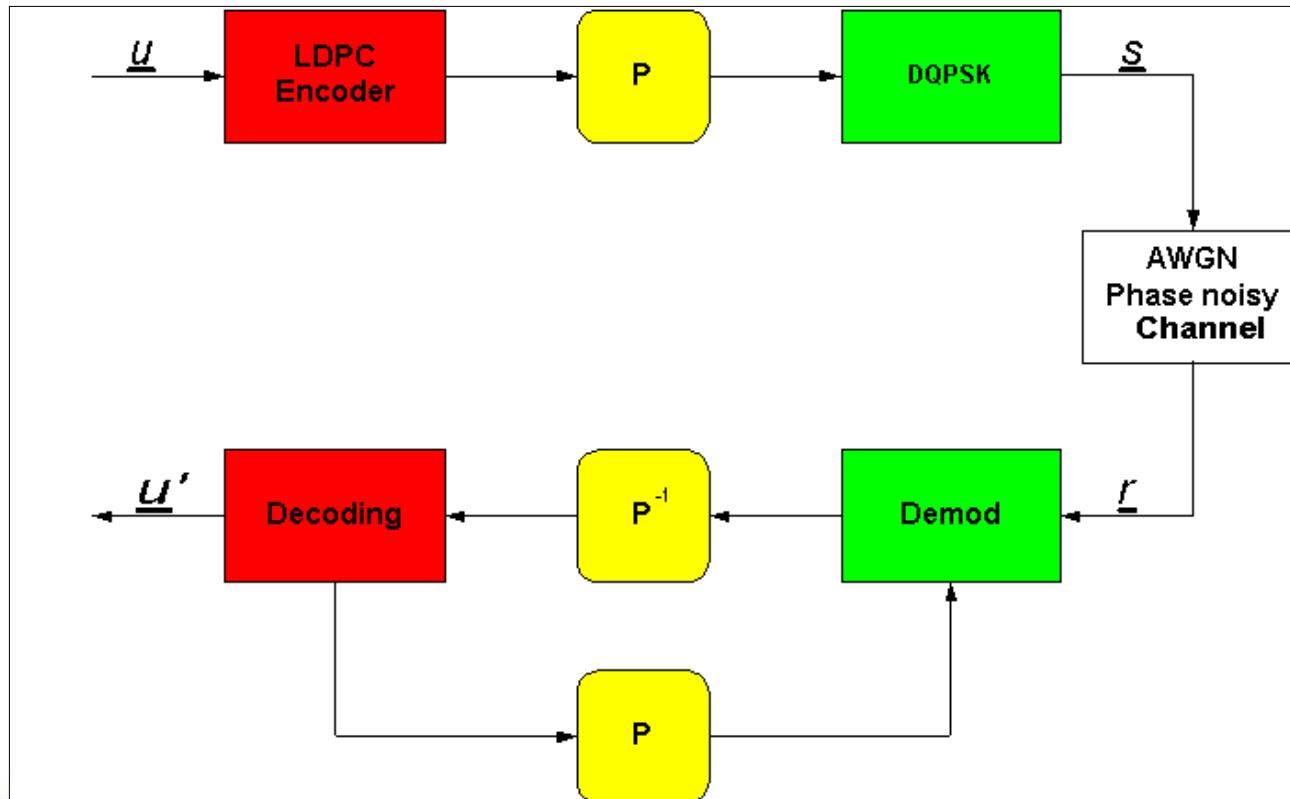


Uplink Modulation

- Differentially encoded QPSK
- Dwell structured transmission



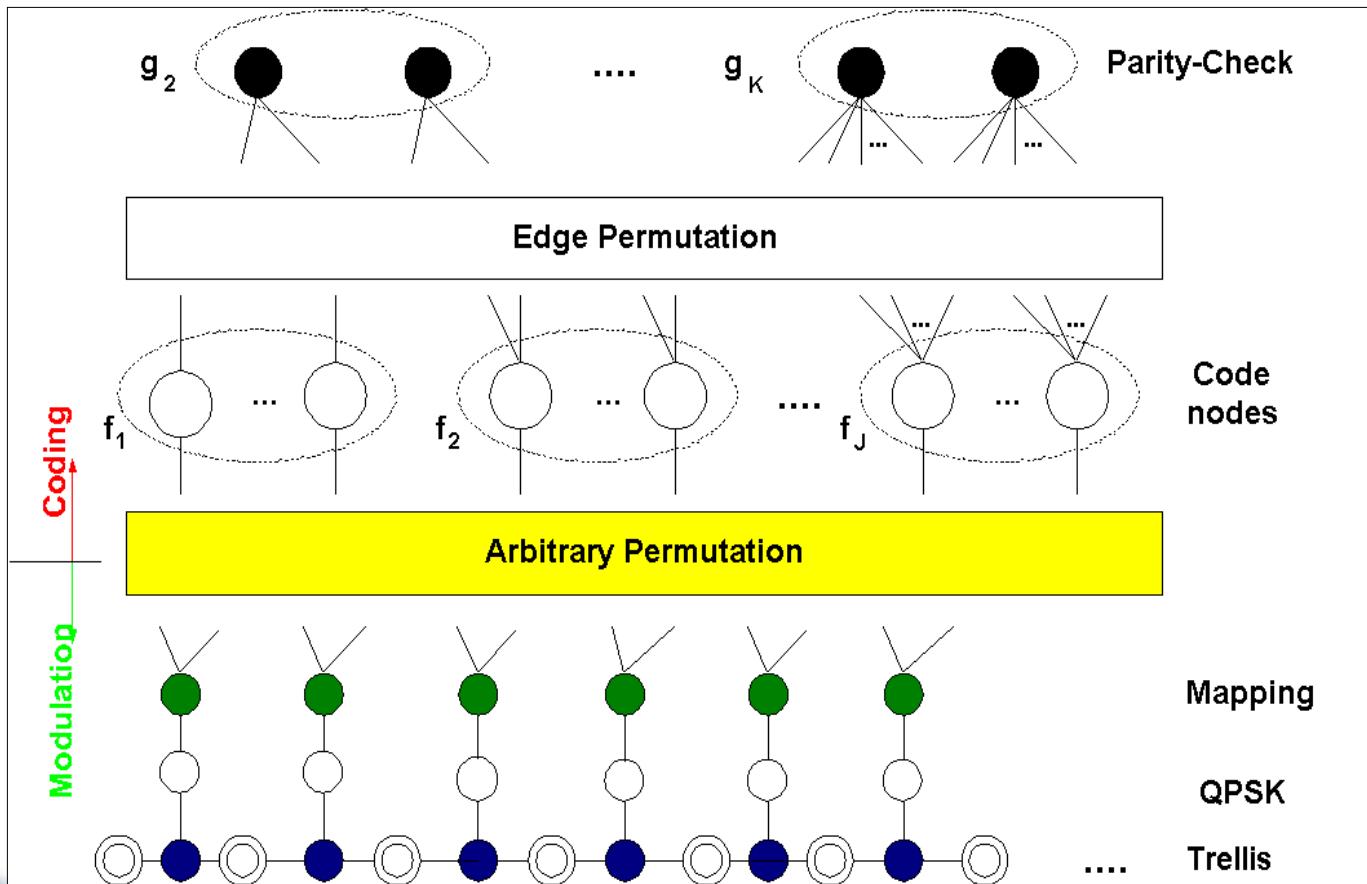
Baseband (Flat) Model



Channel Model: $r_i = e^{j\theta} s_i + n_i$



Graph Representation



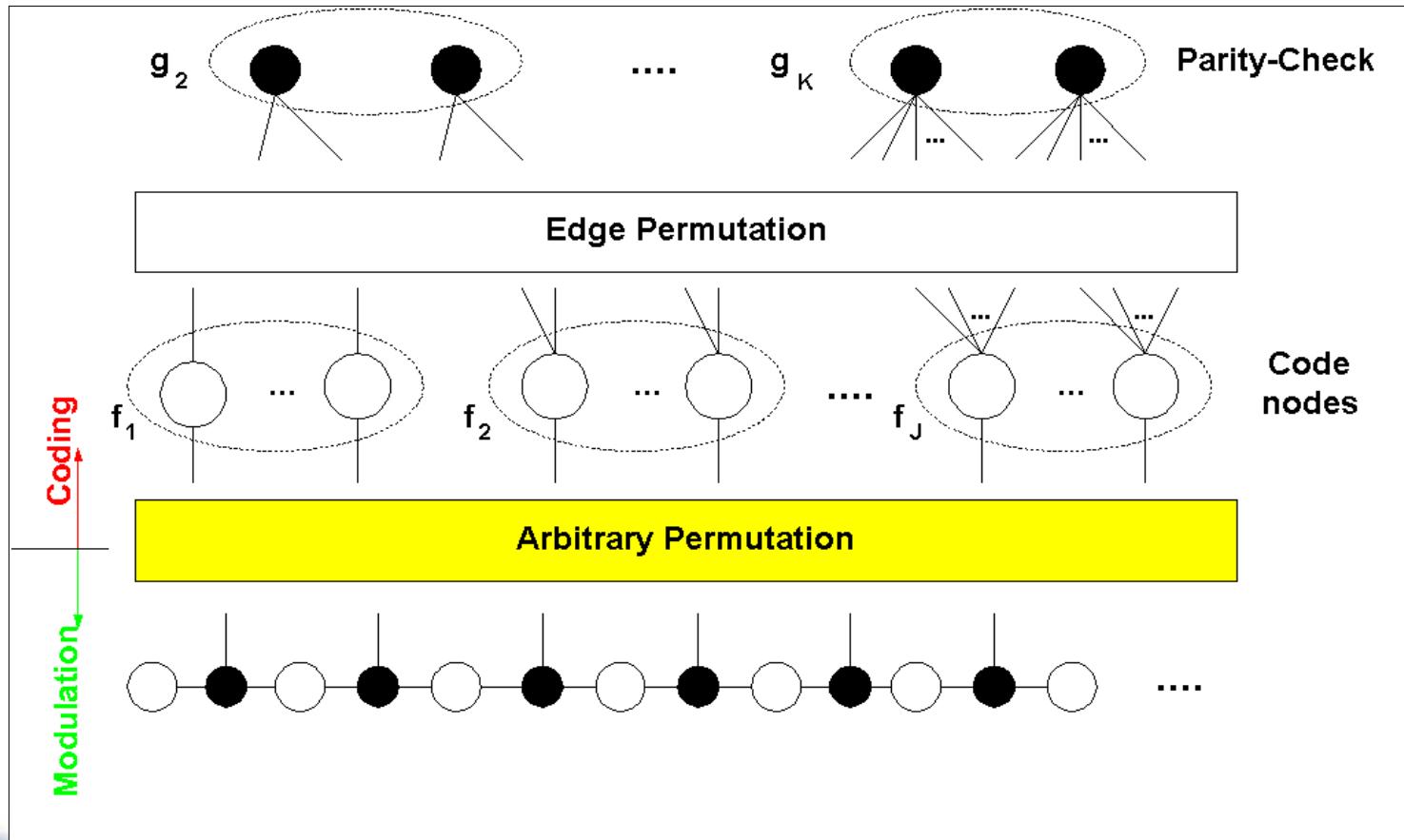
Simplified Model

- BPSK signaling.
- Unknown phase can only be 0 or π with equal probability.

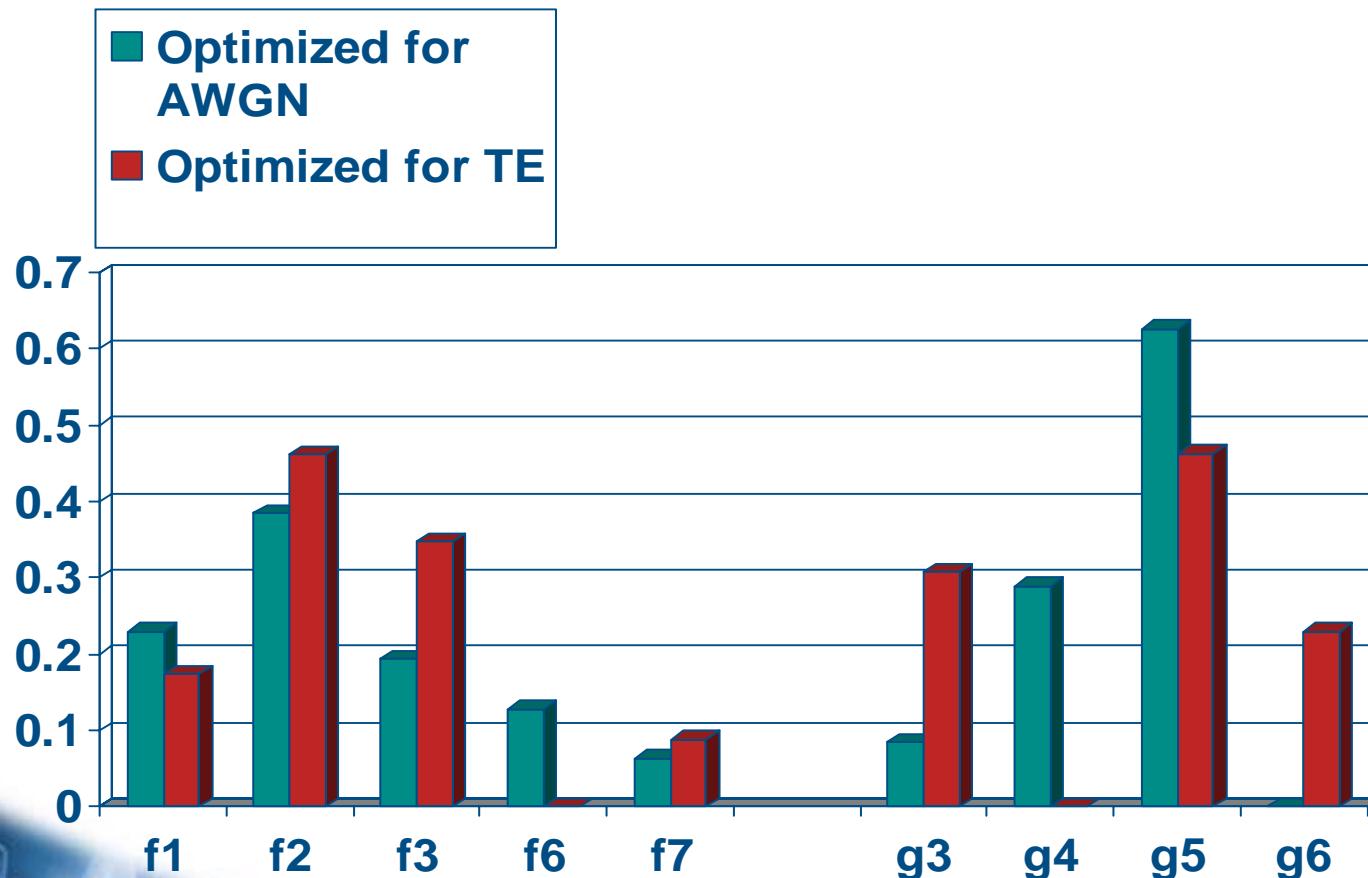
$$r_i = z s_i + n_i, \quad z = \{-1, +1\}.$$



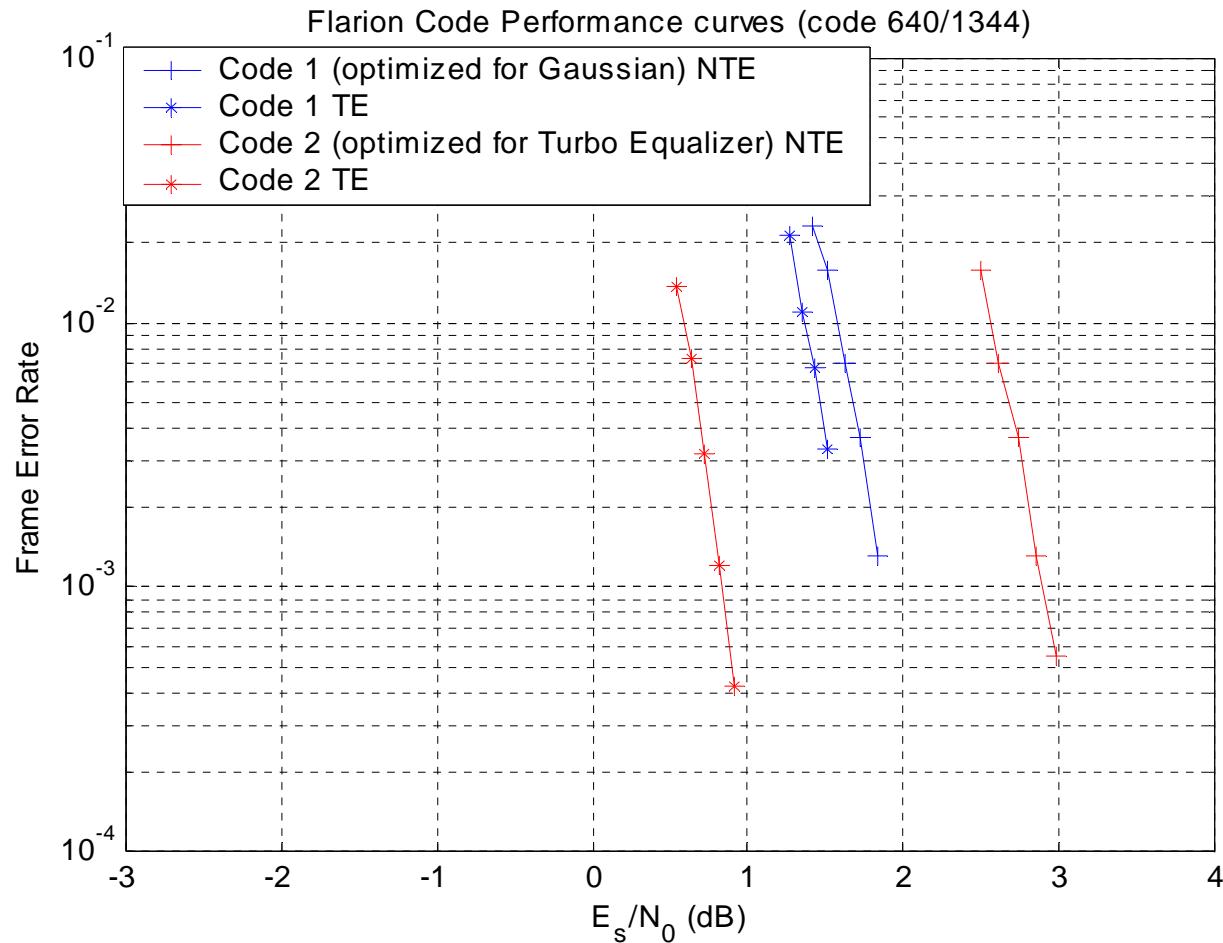
Tanner Graph of Simplified Model



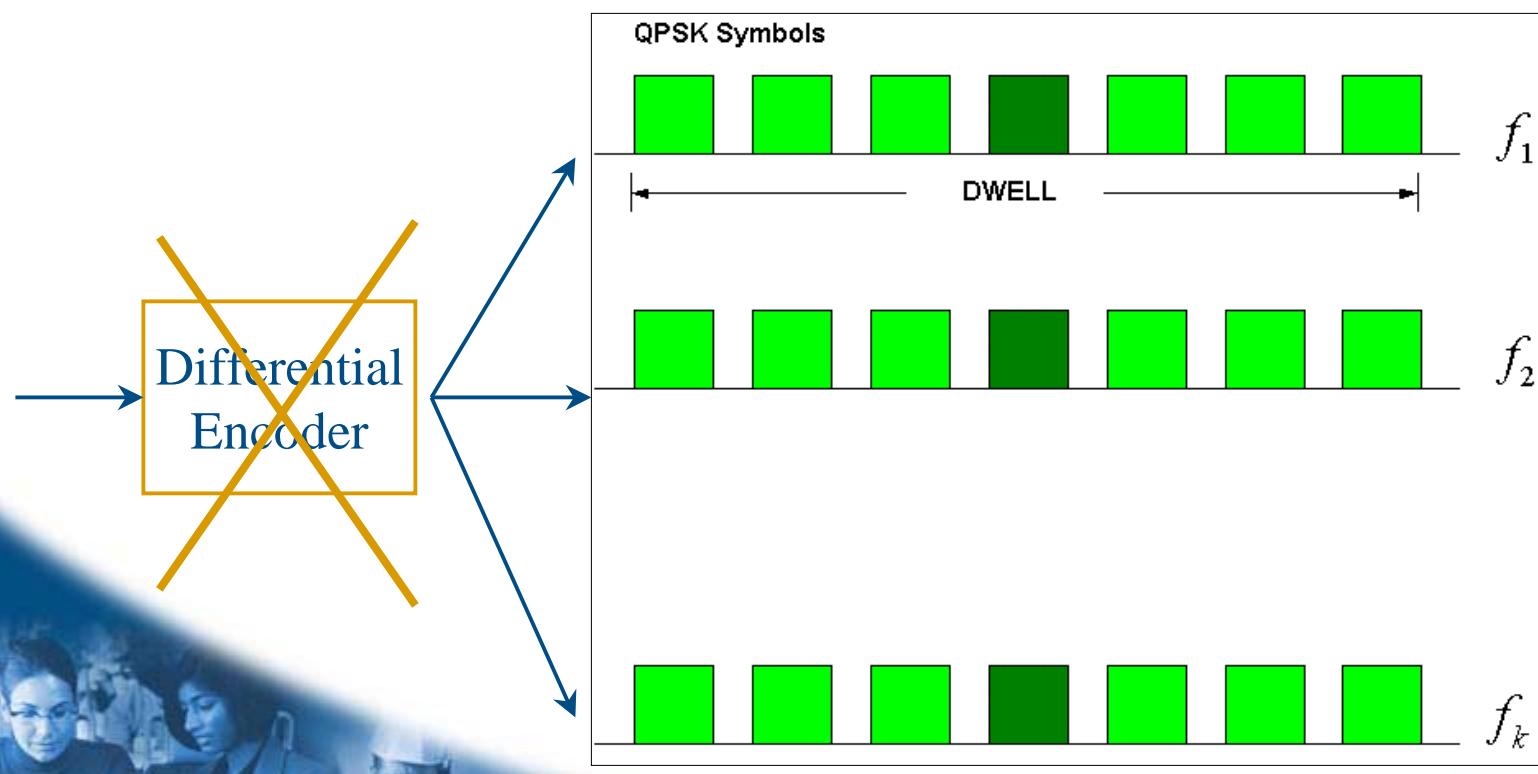
Optimized Degree Profile



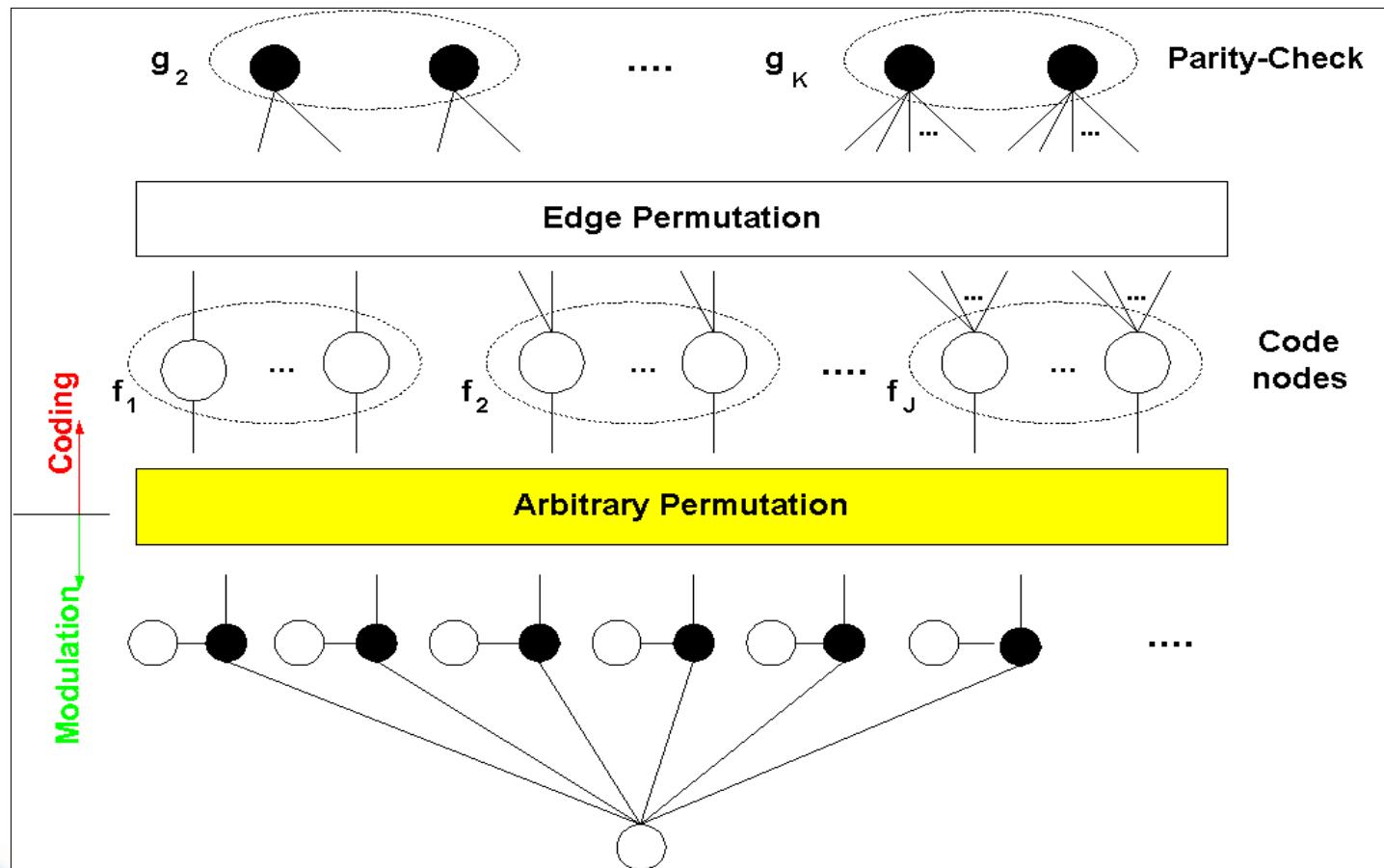
Performance



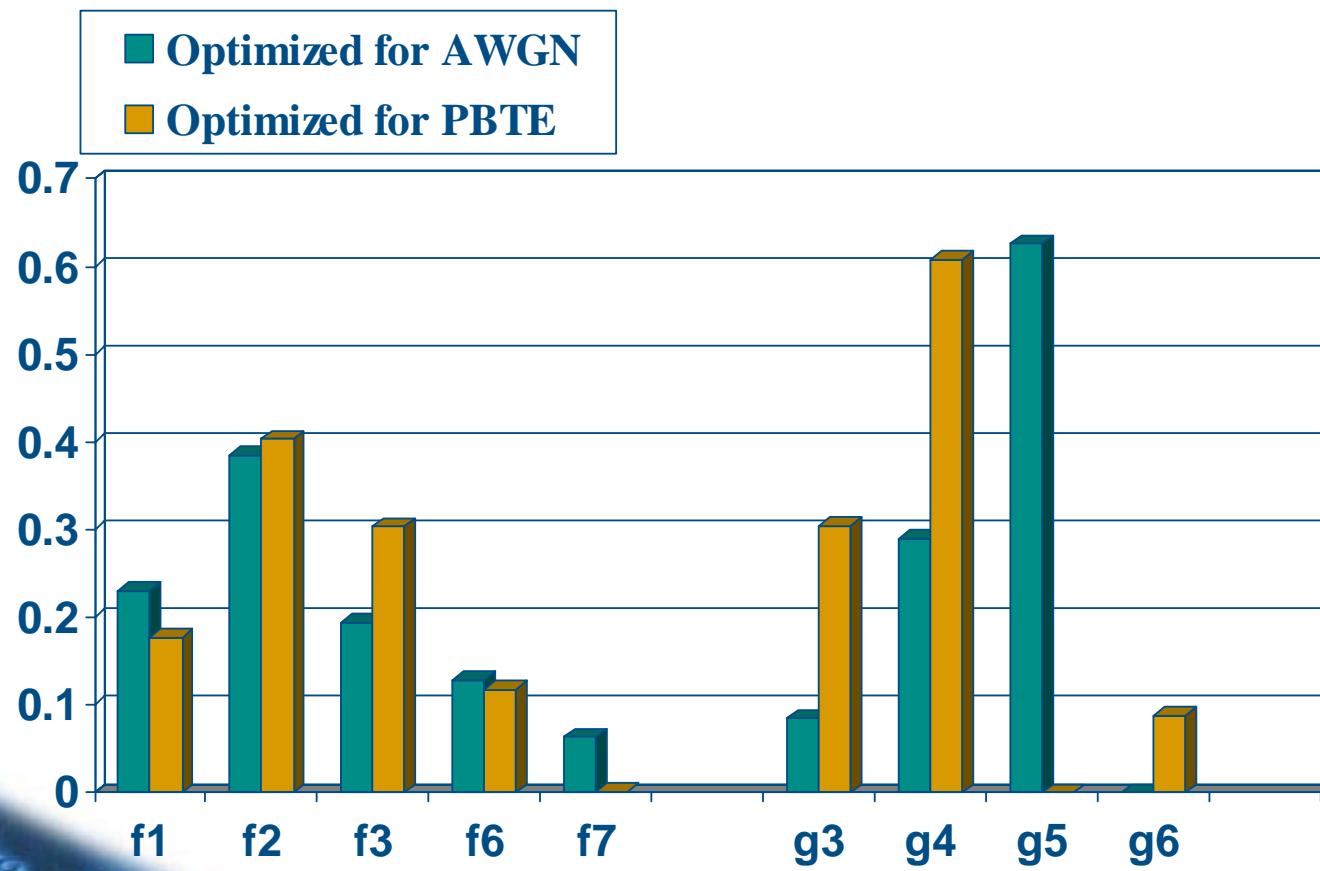
New Modulation Scheme



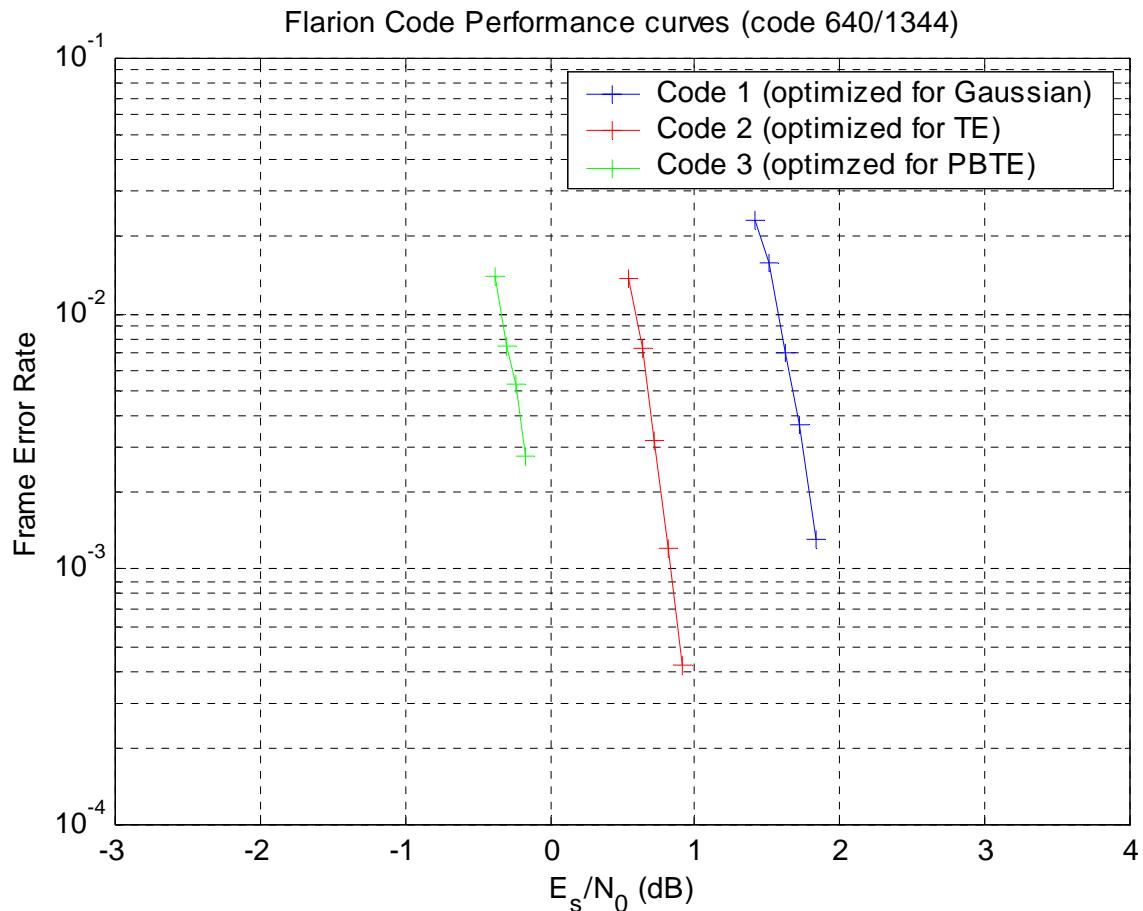
Tanner Graph (Again)



Optimized Degree Profile

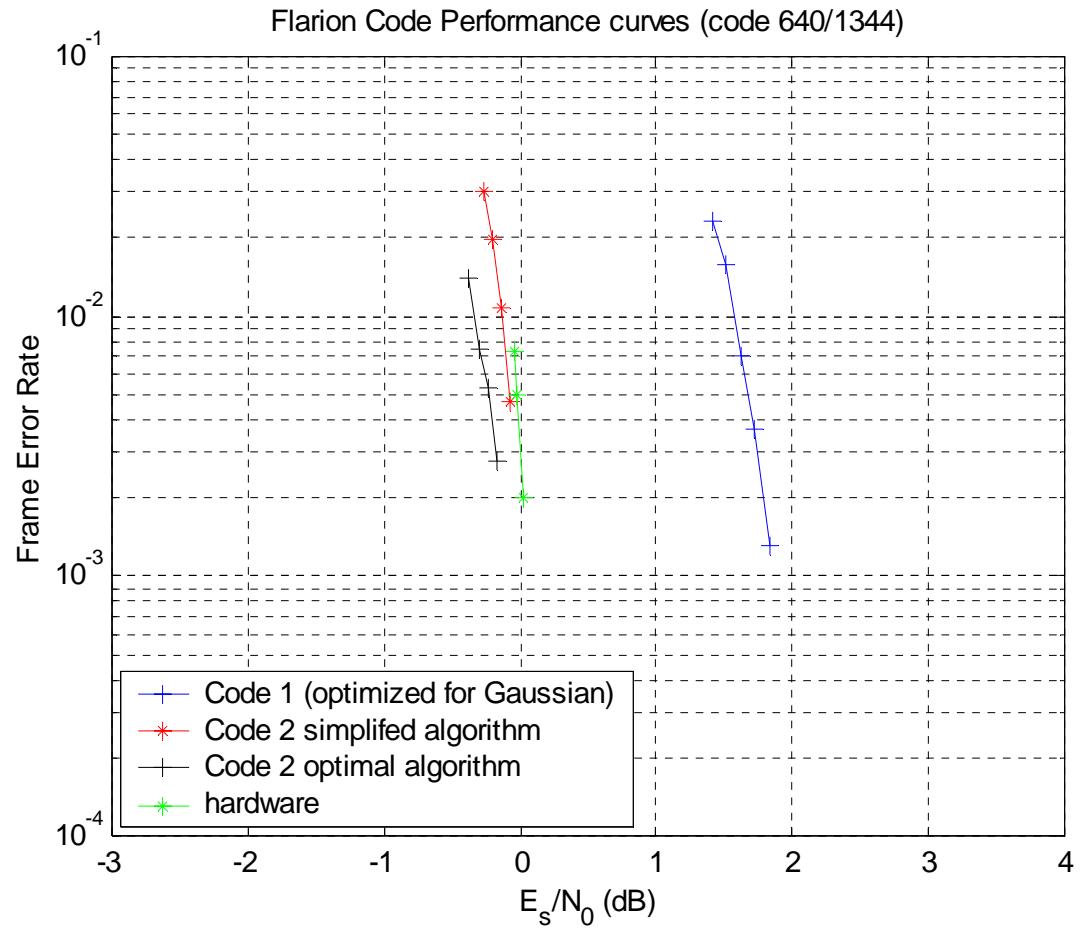


Performance



Simplified Algorithm

Approximate MAP
decision in
demodulation
Similar to a complex
check node
update.



Hardware Implementation

- Less than 50% complexity increase, compared with decoder alone.
- Runs at over 100 MHz on Xilinx VirtexE 2000.



Summary

- LDPC codes design in conjunction with turbo equalizer
- Hardware implemented algorithm with 1.7 dB performance gain

